

## CLAIMS

### WHAT IS CLAIMED IS:

- 1                    1.     A method of manufacturing an integrated circuit, the  
2     method comprising:  
3                    providing a first gate structure and a second gate structure  
4     on a semiconductor substrate including a strained semiconductor layer,  
5     the first gate structure and the second gate structure each including a  
6     first spacer, wherein the first gate structure is provided above a first area  
7     of the strained semiconductor layer and the second gate structure is  
8     provided above a second area of the strained semiconductor layer;  
9                    providing a first masking layer above the first area;  
10                   forming first deep source and drain regions in the strained  
11     semiconductor layer in the second area;  
12                   removing the first masking layer;  
13                   masking the second area with a second masking layer;  
14                   providing a second spacer to the first gate structure; and  
15                   forming second deep source and drain regions in the strained  
16     semiconductor layer in the second area.
- 1                    2.     The method of claim 1, further comprising:  
2                    activating the first and second deep source and drain regions  
3     in an annealing process.
- 1                    3.     The method of claim 2, wherein the annealing process  
2     operates at less than 600°C.
- 1                    4.     The method of claim 3, wherein the removing step is a  
2     dry-etching step.
- 1                    5.     The method of claim 4, wherein the first and second  
2     spacers comprise nitride.
- 1                    6.     The method of claim 1, further comprising:

2                   siliciding the first and second gate structures and the first  
3                   and second source and drain regions.

1                   7.     The method of claim 1, wherein the first and second  
2                   gate structures includes a polysilicon conductor.

1                   8.     The method of claim 1, further comprising:  
2                   covering at least a portion of the semiconductor substrate  
3                   with an insulative layer.

1                   9.     The method of claim 1, wherein the second spacers  
2                   are approximately 500 angstroms wide.

1                   10.    The method of claim 9, wherein the second source  
2                   and drain regions include Arsenic.

1                   11.    A method of manufacturing an ultra-large scale  
2                   integrated circuit including a plurality of field effect transistors having  
3                   gate structures, the method comprising the steps of:  
4                   selectively providing deep source and drain regions for a first  
5                   group of the field effect transistors;  
6                   selectively providing offset spacers for a second group of the  
7                   field effect transistors, the second group of the field effect transistors  
8                   being different than the first group of the field effect transistors, wherein  
9                   the first group and the second group are provided on a top surface of a  
10                  strained semiconductor layer; and  
11                  selectively providing source and drain regions for the second  
12                  group.

1                   12.    The method of claim 11, further comprising:  
2                   providing a silicide layer above the source and drain regions  
3                   for the first group and the second group.

1                   13.    The method of claim 12, further comprising:  
2                   providing a silicon dioxide layer over the silicide layer.

1                   14.    The method of claim 11, wherein the strained  
2   semiconductor layer includes silicon.

1                   15.    The method of claim 14, wherein the silicon is above a  
2   silicon/germanium layer.

1                   16.    The method of claim 15, wherein the offset spacers  
2   are approximately 500-2000 angstroms high and approximately 500  
3   angstroms wide.

1                   17.    A process of forming source and drain regions on a  
2   semiconductor substrate, the process comprising:  
3                   forming a plurality of gate structures on a top surface of a  
4   strained silicon layer;  
5                   covering a first set of gate structures;  
6                   forming deep source and drain regions on each side of a  
7   second set of the gate structures;  
8                   uncovering the first set of gate structures;  
9                   covering the second set of gate structures;  
10                  providing spacers for the first set of gate structures; and  
11                  forming deep source and drain regions on each side of the  
12   first set of the gate structures.

1                   18.    The process of claim 17, further comprising:  
2                   annealing the strained silicon layer after the providing steps.

1                   19.    The process of claim 18, wherein the strained silicon  
2   layer is provided above a silicon germanium layer.

1                   20.    The process of claim 19, wherein the deep source and  
2   drain regions are provided by ion implantation.